

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-3. (Canceled)

1 4. (Currently Amended) A method for synchronizing a digital video host
2 system including a host computer; a receiver circuit and a decoder circuit ~~coupled with the~~
3 ~~receiver circuit only through a host system bus~~; the method comprising:
4 (a) coupling the receiver circuit with the decoder circuit only through separate
5 nodes of a bus in the host computer;
6 (b)(a) receiving a first transport packet from a transmitter with the receiver
7 circuit;
8 (c)(b) capturing a first system time clock (STC) timestamp at a start of receiving
9 the first transport packet, the first STC timestamp being captured into a latch;
10 (d)(e) obtaining a program clock reference (PCR) timestamp from the transport
11 packet;
12 (e)(d) comparing the first STC timestamp to the PCR timestamp to generate a
13 comparison result;
14 (f)(e) adjusting an STC frequency based on the comparison result in order to
15 maintain synchronization between the receiver circuit and the transmitter;
16 (g)(f) capturing, with the decoder circuit, a system timestamp for an application
17 system coupled with the decoder circuit but not with the receiver circuit; and
18 (h)(g) adjusting the system timestamp with an offset based on a message delay
19 time between the decoder circuit and the receiver circuit to maintain synchronization between the
20 decoder circuit and the receiver circuit.

5.-6. (Canceled)

1 7. (Currently amended) The method according to claim 4 further
2 comprising:

3 (a) receiving data from the decoder circuit into a first register in a bus interface
4 on the ~~comprised by the host system~~ bus in the host computer;

5 (b) latching a second STC timestamp into a second register in the bus interface
6 after receiving the data from the decoder circuit; and

7 (c) providing the second STC timestamp to the decoder circuit by way of the
8 second register.

1 8. (Previously presented) The method according to claim 4 wherein the
2 application system comprises an audio-visual system and the decoder circuit comprises an audio-
3 visual interface.

1 9. (Previously presented) The method according to claim 4 wherein the
2 application system comprises a networked computer system and the decoder circuit comprises a
3 computer network interface.

10.-12. (Canceled)

1 13. (Currently Amended) A system for synchronizing a digital video host
2 system including a host computer, a receiver circuit and a decoder circuit ~~coupled with the~~
3 ~~receiver circuit only through a host system bus~~, the system comprising:

4 (a) a bus in the host computer having the receiver circuit and the decoder circuit
5 on separate nodes thereof;

6 (b)(a) a parser adapted to obtain a program clock reference (PCR) timestamp
7 from a first transport packet, the first transport packet including the PCR timestamp;

8 (c)(b) a first latch coupled to the parser, the first latch being adapted to capture a
9 first system time clock (STC) timestamp near a beginning of receipt of a first transport packet
10 from a transmitter by the receiver circuit;

11 (d)(e) a comparison device coupled to the parser and to the latch, the comparison
12 device being configured to compare the STC timestamp to the PCR timestamp so as to generate a
13 comparison result;

14 (e)(d) a first adjuster coupled to the comparison device, the first adjuster being
15 adapted to adjust a frequency of the system time clock based on the comparison result in order to
16 maintain the synchronization between the receiver circuit and the transmitter;

17 (f)(e) a second latch in the decoder circuit, the second latch being adapted to
18 capture a system timestamp for an application system coupled with the decoder circuit but not
19 with the receiver circuit; and

20 (g)(f) a second adjuster coupled to the decoder circuit, the second adjuster being
21 adapted to adjust the system timestamp with an offset based on a message delay time between
22 the decoder circuit and the receiver circuit to maintain synchronization between the decoder
23 circuit and the receiver circuit.

14. – 15. (Canceled).

1 16. (Currently Amended) The system according to claim 13 further
2 comprising:

3 (a) a first register in a bus interface comprised by the ~~host system~~ bus in the host
4 computer, the first register being adapted to receive data from the decoder circuit; and

5 (b) a second register in the bus interface, the second register being adapted to
6 latch a second STC timestamp after the first register receives the data from the decoder circuit,
7 wherein the second STC timestamp is provided to the decoder circuit by way of
8 the second register.

1 17. (Previously presented) The system according to claim 13 wherein the
2 application system comprises an audio-visual system and the decoder circuit comprises an audio-
3 visual interface.

1 18. (Previously presented) The system according to claim 13 wherein the
2 application system comprises a networked computer system and the decoder circuit comprises a
3 computer network interface.

1 19. (Previously presented) The method according to claim 4 wherein the
2 offset is scaled by a nonunity value.

1 20. (Currently amended) A method for synchronizing a digital video host
2 system including a host computer, a receiver circuit and a decoder circuit ~~coupled with the~~
3 ~~receiver circuit only through a host system bus~~, the method comprising:

4 (a) coupling the receiver circuit with the decoder circuit only through a bus in the
5 host computer

6 (b)(a) receiving a first transport packet from a transmitter with the receiver
7 circuit;

8 (c)(b) capturing a first system time clock (STC) timestamp at a start of receiving
9 the first transport packet, the first STC timestamp being captured into a latch;

10 (d)(e) obtaining a program clock reference (PCR) timestamp from the transport
11 packet;

12 (e)(d) comparing the first STC timestamp to the PCR timestamp to generate a
13 comparison result;

14 (f)(e) adjusting an STC frequency based on the comparison result in order to
15 maintain synchronization between the receiver circuit and the transmitter;

16 (g)(f) receiving data from the decoder circuit into a first register in a bus interface
17 comprised by the ~~host system~~ bus in the host computer;

18 (h)(g) latching a second STC timestamp into a second register in the bus interface
19 after receiving the data from the decoder circuit; and

20 (i)(h) providing the second STC timestamp to the decoder circuit by way of the
21 second register.

1 21. (Previously presented) The method according to claim 20 wherein the
2 decoder circuit comprises an audio-visual interface.

1 22. (Previously presented) The method according to claim 20 wherein the
2 decoder circuit comprises a computer network interface.

1 23. (Previously presented) The system according to claim 13 wherein the
2 offset is scaled by a nonunity value.

1 24. (Currently amended) A system for synchronizing a digital video host
2 system including a host computer, a receiver circuit and a decoder circuit ~~coupled with the~~
3 ~~receiver circuit only through a host system bus~~, the system comprising:

4 (a) a bus in the host computer that couples the receiver circuit with the decoder
5 circuit;

6 (b)(a) a parser adapted to obtain a program clock reference (PCR) timestamp
7 from a first transport packet, the first transport packet including the PCR timestamp;

8 ~~(c)~~(b) a first latch coupled to the parser, the first latch being adapted to capture a
9 first system time clock (STC) timestamp near a beginning of receipt of a first transport packet
10 from a transmitter by the receiver circuit;

11 ~~(d)~~(e) a comparison device coupled to the parser and to the latch, the comparison
12 device being configured to compare the STC timestamp to the PCR timestamp so as to generate a
13 comparison result;

14 ~~(e)~~(d) a first adjuster coupled to the comparison device, the first adjuster being
15 adapted to adjust a frequency of the system time clock based on the comparison result in order to
16 maintain the synchronization between the receiver circuit and the transmitter;

17 ~~(f)~~(e) a first register in a bust interface comprised by the host-system bus, the first
18 register being adapted to receive data from the decoder circuit; and

19 ~~(g)~~(f) a second register in the bus interface, the second register being adapted to
20 latch a second STC timestamp after the first register receives the data from the decoder circuit,
21 wherein the second STC timestamp is provided to the decoder circuit by way of the second
22 register.

1 25. (Previously presented) The system according to claim 24 wherein the
2 decoder circuit comprises an audio-visual interface.

1 26. (Previously presented) The system according to claim 24 wherein the
2 decoder circuit comprises a computer network interface.
